

**AMENDMENTS TO THE CLAIMS**

**This listing of claims will replace all prior versions and listings of claims in the application:**

**LISTING OF CLAIMS:**

1. (currently amended): A multi-mode scheduler including a  $N \times kM$  scheduler for adjusting data transmission between  $N$ -pieces of input interface sections, where  $N$  is a positive integer, and said  $kM$ -pieces of output interface sections, where said  $M$  is a positive integer and said  $k$  is an integer not less than two, said multi-mode scheduler comprising:

$k$ -pieces of  $N \times M$  schedulers to be said  $N \times kM$  scheduler; and

$(k-1)$  -pieces of selection circuits for switching allocated output port information input from an outside of said  $N \times kM$  scheduler and information from one of said  $N \times M$  schedulers at a front step so as to be input to another one of said  $N \times M$  schedulers as allocated output port information $[[:]$ ];

wherein an operation of said  $N \times kM$  scheduler or an operation of said  $N \times M$  schedulers having  $k$ -pieces of priority classes is set freely with switching operation of said  $(k-1)$  -pieces of selection circuits.

2. (currently amended): The multi-mode scheduler according to Claim 1, wherein  $j$ -pieces of said  $N \times kM$  scheduler,  $[[()]]$  where  $j$  is an integer not less than two $[[()]]$ , are connected so

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as to make up ~~[[said]]~~ a  $jN \times kM$  scheduler when said allocated output port information input from said outside is used.

3. (original): The multi-mode scheduler according to Claim 2, wherein each of said  $(k-1)$ -pieces of selection circuits selects said allocated output port information input from said outside when said allocated output port information input from said outside is used.

4. (currently amended): The multi-mode scheduler according to Claim 2, wherein  $j$ -pieces of said  $N \times kM$  scheduler are pipeline-connected so as to make up said  $jN \times kM$  scheduler ~~(where  $j$  is an integer not less than two)~~.

5. (currently amended): The multi-mode scheduler according to Claim 1, wherein said  $N \times kM$  scheduler is used alone so as to make up said  $N \times M$  schedulers having  $k$ -pieces of priority classes when information from said  $N \times M$  scheduler at said front step is used.

6. (currently amended): The multi-mode scheduler according to Claim 5, wherein each of said  $(k-1)$ -pieces of selection circuits selects information from one of said  $N \times M$  schedulers at said front step when said  $N \times kM$  scheduler is used alone.

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7. (currently amended): The multi-mode scheduler according to Claim 1, wherein each of said N-pieces of input interface sections includes a virtual output queue[[]] buffer for storing reception data for each output interface section to be a destination.

8. (currently amended): A multi-mode scheduler including a N x kM scheduler for adjusting data transmission between N-pieces of input interface means, where [[said]] N is a positive integer, and said kM-pieces of output interface means, where said M is a positive integer and said k is an integer not less than two, said multi-mode scheduler comprising:

k-pieces of N x M schedulers to be said N x kM scheduler; and

(k-1)-pieces of selection means for switching allocated output port information input from an outside of said N x kM scheduler and information from one of said N x M schedulers at a front step so as to be input to another one of said N x M schedulers as allocated output port information[[:]];

wherein an operation of said N x kM scheduler or an operation of said N x M schedulers having k-pieces of priority classes is set freely with switching operation of said (k-1) -pieces of selection means.

9. (currently amended): The multi-mode scheduler according to Claim 8, wherein j-pieces of said N x kM scheduler, [[()]]where j is an integer not less than two[[]], are connected so

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as to make up ~~[[said]]~~ a  $jN \times kM$  scheduler when said allocated output port information input from said outside is used.

10. (original): The multi-mode scheduler according to Claim 9, wherein each of said (k-1) -pieces of selection means selects said allocated output port information input from said outside when said allocated output port information input from said outside is used.

11. (currently amended): The multi-mode scheduler according to Claim 9, wherein j-pieces of said  $N \times kM$  scheduler are pipeline-connected so as to make up said  $jN \times kM$  scheduler ~~(where j is an integer not less than two)~~.

12. (currently amended): The multi-mode scheduler according to Claim 8, wherein said  $N \times kM$  scheduler is used alone so as to make up said  $N \times M$  schedulers having k-pieces of priority classes when information from said  $N \times M$  scheduler at said front step is used.

13. (currently amended): The multi-mode scheduler according to Claim 12, wherein each of said (k-1)-pieces of selection means selects information from one of said  $N \times M$  schedulers at said front step when said  $N \times kM$  scheduler is used alone.

14. (currently amended): The multi-mode scheduler according to Claim 8, wherein each of said N-pieces of input interface means includes a virtual output queue[[]] buffer for storing reception data for each output interface means to be a destination.

15. (currently amended): An apparatus including a multi-mode scheduler including a  $N \times kM$  scheduler for adjusting data transmission between N-pieces of input interface sections, where N is a positive integer, and kM-pieces of output interface sections, where M is a positive integer and k is an integer not less than two, ~~said multi-mode scheduler~~ comprising:

k-pieces of  $N \times M$  schedulers to be said  $N \times kM$  scheduler; and

(k-1) -pieces of selection circuits for switching allocated output port information input from an outside of said  $N \times kM$  scheduler and information from one of said  $N \times M$  schedulers at a front step so as to be input to another one of said  $N \times M$  schedulers as allocated output port information[[:]];

wherein an operation of said  $N \times kM$  scheduler or an operation of said  $N \times M$  schedulers having k-pieces of priority classes is set freely with switching operation of said (k-1) -pieces of selection circuits.

16. (currently amended): An apparatus including a multi-mode scheduler including a  $N \times kM$  scheduler for adjusting data transmission between N-pieces of input interface means,

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where N is a positive integer, and kM-pieces of output interface means, where M is a positive integer and k is an integer not less than two, ~~said multi-mode scheduler~~ comprising:

k-pieces of N x M schedulers to be said N x kM scheduler; and

(k-1)-pieces of selection means for switching allocated output port information input from an outside of said N x kM scheduler and information from one of said N x M schedulers at a front step so as to be input to another one of said N x M schedulers as allocated output port information[[:]];

wherein an operation of said N x kM scheduler or an operation of said N x M schedulers having k-pieces of priority classes is set freely with switching operation of said (k-1)-pieces of selection means.

17. (currently amended): A multi-mode scheduling method used in a N x kM scheduler for adjusting data transmission between N-pieces of input interface means, where N is a positive integer, and kM-pieces of output interface means, where M is a positive integer and k is an integer not less than two, ~~said multi-mode scheduler~~ comprising:

forming said N x kM scheduler from k-pieces of N x M schedulers ~~to be said N x kM scheduler~~; and

switching, in (k-1)-pieces of selection circuits, ~~for switching~~ allocated output port information input from an outside of said N x kM scheduler and information from one of said N

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x M schedulers at a front step so as to be input to another one of said N x M schedulers as  
allocated output port information[[:]];

wherein an operation of said N x kM scheduler or an operation of said N x M schedulers  
having k-pieces of priority classes is set freely with switching operation of said (k-1) -pieces of  
selection circuits.